UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/423,415	11/05/1999	SEISUKE MORIOKA	27877.00066	6706

7590 06/09/2005

JOSEPH R KEATING,ESQ
KEATING & BENNETT,LLP
10400 EATON PLACE SUITE 312
FAIRFAX, VA 22030

EXAMINER	
BLACKMAN, ANTHONY J	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/423,415	MORIOKA, SEISUKE	
	Examiner	Art Unit	
	ANTHONY J BLACKMAN	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-20 and 22-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-20 and 22-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 11/24/04 has been entered.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 11/24/04 is being considered by the examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11-17, 22-23, 26-31 and 34 rejected under 35 U.S.C. 103(a) as being unpatentable over The A.G.P. Interface Specification Revision 1.0 by INTEL from July 31, 1996 (referred to as INTEL) in view of DYE, US Patent No. 6,370,631.

5. As per claim 14 , examiner interprets INTEL to disclose an apparatus for image processing (see figures 1-1, 2-2 and 2-3) comprising:; a first storage device having texture data and electronically coupled to said processor; wherein transmission of texture data between said texture buffer and said processor is faster than transmission of texture data (inherent use of texture data is disclosed throughout section 1.1 Motivation, therefore, the LFB is a texture buffer) between said storage device and said processor (see fig 1-1, the local frame buffer-LFB is analogous to the storage device and the AGP itself represents the faster transmission between storage and the processor (analogous to the CPU)) ; and said first storage device is defined by a CPU work memory or an external memory device (it is inherent that the LFB is defined by the processor (analogous to the CPU), however, INTEL does not expressly teach a processor including a data decompression circuit as claimed.

DYE discloses a memory controller (IMC) and the IMC Block Diagram (see col 12, line 64) discloses FIFO means, codec engine, and texture mapping logic respectively (see col 13, lines 11-24 and for further explanation of the IMC codec means see col 15, lines 23-41 and and col 16, lines 11-13 representing the processor above as claimed). It would have been obvious to one skilled in the art at the time of the invention to utilize the memory controller (IMC) for specialized codec engine means of DYE to modify the AGP Interface teaching as disclosed above of INTEL because use of the codec engine of DYE provides (1) improved performance (see col 2, lines 40-44); (2) the IMC also improves overall system performance and response using main system memory for

graphical information and storage and also reduces bandwidth requirements for graphical displays (see col 2, lines 52-67).

6. As per claim 11, INTEL as modified meets limitations of claim 14, INTEL further discloses, comprising a frame buffer, wherein said processor stores image data in said frame buffer (see section 2.1, second paragraph, lines 1-4).

7. As per claim 12, INTEL as modified meets limitations of claim 14, wherein said processor reads decompressed texture data contained in said texture buffer (inherent use of texture data is disclosed throughout section 1.1 Motivation, therefore, the LFB is a texture buffer), however, does not expressly teach and performs image processing of said decompressed texture data for conversion to image data. DYE teaches and performs image processing of said decompressed texture data for conversion to image data (see above; codec engine, and texture mapping logic respectively, wherein the codec engine performs functions representative of the claimed function (see col 13, lines 11-24 and for further explanation of the IMC codec means see col 15, lines 23-41 and and col 16, lines 11-13). It would have been obvious to one skilled in the art at the time of the invention to utilize the memory controller (IMC) for specialized codec engine means of DYE to modify the AGP Interface teaching as disclosed above of INTEL because use of the codec engine of DYE provides (1) improved performance (see col 2, lines 40-44); (2) the IMC also improves overall system performance and response using main system memory for graphical information and storage and also reduces bandwidth requirements for graphical displays (see col 2, lines 52-67).

8. As per claim 13, INTEL as modified meet limitations of claim 14, INTEL does not expressly teach the following, wherein said processor reads compressed texture data from said first storage device, said data decompression circuit decompresses said read compressed texture data, and said processor stores said decompressed texture data in said texture buffer. DYE teach the codec engine means (col 13, lines 11-24) representative of wherein said processor reads compressed texture data from said first storage device, said data decompression circuit decompresses said read compressed texture data, and said processor stores said decompressed texture data in said texture buffer). It would have been obvious to one skilled in the art at the time of the invention to utilize the memory controller (IMC) for specialized codec engine means of DYE to modify the AGP Interface teaching as disclosed above of INTEL because use of the codec engine of DYE provides (1) improved performance (see col 2, lines 40-44); (2) the IMC also improves overall system performance and response using main system memory for graphical information and storage and also reduces bandwidth requirements for graphical displays (see col 2, lines 52-67).

9. As per claim 15, claim 15 is substantially similar to claim 14, claim 15 adds data buses associated with the processor. These features are claimed and he INTEL processor means reads on the features (see fig 1 showing the AGP on one side of the chipset and the other, slower bus from sys mem).

10. As per claim 16, INTEL as modified meets limitations of claim 13, however, INTEL does not expressly teach wherein said processor including a FIFO storage device temporarily stores said read compressed texture data. DYE teaches wherein said processor including a FIFO storage device temporarily stores said read compressed texture data discloses FIFO means, codec engine, and texture mapping logic respectively (see col 13, lines 11-24 and for further explanation of the IMC codec means see col 15, lines 23-41 and and col 16, lines 11-13). It would have been obvious to one skilled in the art at the time of the invention to utilize the memory controller (IMC) for specialized codec engine means of DYE to modify the AGP Interface teaching as disclosed above of INTEL because use of the codec engine of DYE provides (1) improved performance (see col 2, lines 40-44); (2) the IMC also improves overall system performance and response using main system memory for graphical information and storage and also reduces bandwidth requirements for graphical displays (see col 2, lines 52-67).

11. As per claim 17, INTEL as modified meet limitations of claim 16, INTEL does not expressly teach, wherein said data decompression circuit receives said read compressed data from said storage device. DYE discloses the codec engine suggesting the IMC codec means (see col 15, lines 23-41 and and col 16, lines 11-13). It would have been obvious to one skilled in the art at the time of the invention to utilize the memory controller (IMC) for specialized codec engine means of DYE to modify the AGP Interface teaching as disclosed above of INTEL because use of the codec engine of

DYE provides (1) improved performance (see col 2, lines 40-44); (2) the IMC also improves overall system performance and response using main system memory for graphical information and storage and also reduces bandwidth requirements for graphical displays (see col 2, lines 52-67).

12. As per claim 20, INTEL as modified meet limitations of 14, however, INTEL does not teach, wherein said texture data in said first storage device is compressed . DYE suggests wherein said texture data in said storage device is compressed (the IMC codec means (see col 15, lines 23-41 and and col 16, lines 11-13). It would have been obvious to one skilled in the art at the time of the invention to utilize the memory controller (IMC) for specialized codec engine means of DYE to modify the AGP Interface teaching as disclosed above of INTEL because use of the codec engine of DYE provides (1) improved performance (see col 2, lines 40-44); (2) the IMC also improves overall system performance and response using main system memory for graphical information and storage and also reduces bandwidth requirements for graphical displays (see col 2, lines 52-67).

13. As per claim 23, is substantially similar to both claims 14 and 15. DYE's IMC codec means discloses the following limitation not expressly taught in claim 14 or 15 reading said compressed texture data in a storage device (the IMC codec means (see col 15, lines 23-41 and col 16, lines 11-13).

14. As per claim 22, INTEL as modified meets limitations of claim 23, INTEL does not expressly teach further comprising the step of converting said decompressed texture data to image data, and storing said image data, and storing said image data in a frame buffer. DYE disclose teach further comprising the step of converting said decompressed texture data to image data, and storing said image data, and storing said image data in a frame buffer (see fig 14, col 3, lines 1-10 and col 20, lines 31-49). It would have been obvious to one skilled in the art at the time of the invention to utilize the memory controller (IMC) for specialized codec engine means of DYE to modify the AGP Interface teaching as disclosed above of INTEL because use of the codec engine of DYE provides (1) improved performance (see col 2, lines 40-44); (2) the IMC also improves overall system performance and response using main system memory for graphical information and storage and also reduces bandwidth requirements for graphical displays (see col 2, lines 52-67).

15. As per claim 26, INTEL as modified meet limitations of claim 23. INTEL does not expressly teach wherein the step of storing said decompressed texture data includes the step of updating said decompressed texture data includes the step of updating said decompressed texture data in said texture buffer with new decompressed texture data. DYE teach wherein the step of storing said decompressed texture data includes the step of updating said decompressed texture data includes the step of updating said decompressed texture data in said texture buffer with new decompressed texture data (see col 17, lines 45-67 where the updating is analogous to refreshing).). It would

have been obvious to one skilled in the art at the time of the invention to utilize the memory controller (IMC) for specialized codec engine means of DYE to modify the AGP Interface teaching as disclosed above of INTEL because use of the codec engine of DYE provides (1) improved performance (see col 2, lines 40-44); (2) the IMC also improves overall system performance and response using main system memory for graphical information and storage and also reduces bandwidth requirements for graphical displays (see col 2, lines 52-67).

16. As per claim 27, claim 27 is substantially similar to claim 11.

17. As per claim 28, claim 28 is substantially similar to claim 12.

18. As per claim 29, claim 29 is substantially similar to claim 13.

19. As per claim 30, claim 30 is substantially similar to claim 16.

20. As per claim 31, claim 31 is substantially similar to claim 17.

21. As per claim 34, claim 34 is substantially similar to claim 20.

22. Claims 11-17, 22-23, 26-31 and 34 rejected under 35 U.S.C. 103(a) as being unpatentable over The A.G.P. Interface Specification Revision 1.0 by INTEL from July 31, 1996 (referred to as INTEL) in view of DYE, US Patent No. 6,370,631 and further in view of LENTZ , US Patent No. 5,649,173.

23. As per claims 18, 24 and 32, INTEL as modified meet limitations and features of claims 13, 23 and 29, however, do not expressly teach wherein said processor includes a palette transformation circuit, said palette transformation circuit performing palette transformation of said decomposed texture data. COSMAN et al provides teaching that bear similar results to the limitations as claimed, wherein said processor includes a palette transformation circuit, said palette transformation circuit performing palette transformation of said decomposed texture data (col 6, lines 44-67 teach a prefiltering means that "involves decomposing a color texture map-image (the color texture map-image is analogous to the palette associated with the decomposed texture)). It would have been obvious to one skilled in the art at the time of the invention to use the prefiltering approach described above, including use of the geometry processor or texture processor and also the rendering processor to provide clipping , lighting, texture mapping calculations and other geometry transformations (col 6, lines 57-63) of LENTZ (HARDWARE ARCHITECHTURE FOR IMAGE GENERATION AND MANIPULATION) to modify the 3d graphical display of the Accelerated Graphics Port (AGP) of INTEL as modified because the addition of LENTZ provides detailed rendering features applying

further filter operations (providing greater detail, such as tri-linear filtering – see col 6, lines 48-53). Therefore, because the teachings of LENTZ provide detailed filtering including clipping , lighting, texture mapping calculations and other geometry transformations, it would have been obvious to modify the already INTEL as modified by LENTZ for more detailed filtering texture filtering.

24. As per claims 19, 25 and 33, INTEL as modified meet limitations and features of claims 13, 23 and 29, however, do not expressly teach wherein said processor includes a mip map generation circuit, said mip map generation circuit generating a mip map of said decompressed data. LENTZ suggest wherein said processor includes a mip map generation circuit, said mip map generation circuit generating a mip map of said decompressed data (col 6, lines 44-67 teach a prefiltering means that "involves decomposing a color texture map-image (the color texture map-image is analogous to the palette associated with the decomposed texture)). It would have been obvious to one skilled in the art at the time of the invention to use the prefiltering approach described above, including use of the geometry processor or texture processor and also the rendering processor to provide clipping , lighting, texture mapping calculations and other geometry transformations (col 6, lines 57-63) of LENTZ (HARDWARE ARCHITECHTURE FOR IMAGE GENERATION AND MANIPULATION) to modify the 3d graphical display of the Accelerated Graphics Port (AGP) of INTEL as modified because the addition of LENTZ provides detailed rendering features applying further filter operations (providing greater detail, such as tri-linear filtering – see col 6, lines 48-

53). Therefore, because the teachings of LENTZ provide detailed filtering including clipping , lighting, texture mapping calculations and other geometry transformations, it would have been obvious to modify the already INTEL as modified by LENTZ for more detailed filtering texture filtering.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. COSMAN, US Patent No. 5,734,386 texel mip-map filtering column 6 and see figure 1. .

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANTHONY J BLACKMAN whose telephone number is 571-272-7779. The examiner can normally be reached on FLEX SCHEDULE.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MATTHEW BELLA can be reached on 571-272-7778. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANTHONY J BLACKMAN
Examiner
Art Unit 2676

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600